U.S. UTILITY Patent Application

PATENT NUMBER and ISSUE DATE

I

***APPLICANTS: Randolph Mark; ***CONTINUING DATA VERIFIED: ***Zene** ***Loke** ***PG-FUB DO NOT PUBLISH *** ***PG-FUB DO NOT PUBLISH ** ***PG-FUB DO NOT PUBLISH *** ***PG-FUB DO N			ISCLAMER	WADNIN	C. The informat	- احدثار محد	ed herein may be	- restricte		
***FOREIGN APPLICATIONS VERIFIED: ***TORNEIGN APPLICATIONS VERIFIED: ***TORNEY DOCKET NO ***SUSCISSION ONT PUBLISH *** RESCIND *** ***PRIME DO NOT PUBLISH *** RESCIND *** ***PRIME DO NOT PUBLISH *** RESCIND *** ***PRIME DO NOT PUBLISH *** **		TERMI	NAL	PRE						
*** FOREIGN APPLICATIONS VERIFIED: ***TOREIGN APPLICATIONS VERIFIED: ***John Poly Do Not Publish Programmer	Amo	ount Due D	Date Paid					Figs.Dn	M 0.	Print Fi
*** FOREIGN APPLICATIONS VERIFIED: ***CONTINUING DATA VERIFIED:							DRAWING			
***FOREIGN APPLICATIONS VERIFIED: ***CONTINUING DATA VERIFIED: ***TORE CONTINUING DATA VERIFIED: ***Loke** ***POREIGN APPLICATIONS VERIFIED: ***Loke** PG-PUB DC NOT PUBLISH ** **POREIGN APPLICATIONS VERIFIED: ***Loke** PG-PUB DC NOT PUBLISH ** Priving publify claimed 35 USC 119 conditions met 35 USC 119 conditions met 35 USC 119 conditions met 37 USC 119 Conditions met 38 USC 119 Conditions met 39 USC 119 Conditions met 39 USC 119 Conditions met 30727/2243P **TITLE : Planar transistor structure using isolation implants for improved Vss resistance and for process simplification US DEPT. OF COMM MATS TAMPIC-DEBURG: 12-24			· · · · · · · · · · · · · · · · · · ·	Assistant	Examiner		Total Claims			Ctaim fo
**FOREIGN APPLICATIONS VERIFIED: **TOREIGN APPLICATIONS VERIFIED: **TORE	ЮТІ	ICE OF ALLOW/	ANCE MAILED				CLA	IMS ALL	OWE	Dog
***FOREIGN APPLICATIONS VERIFIED: ***ZONE							· · · · · · · · · · · · · · · · · · ·			·
***APPLICANTS: Randolph Mark; ***CONTINUING DATA VERIFIED: ***TOREIGN APPLICATIONS VERIFIED: ***Loke** PG-PUB DO NOT PUBLISH ** Priving priority claimed	ľ				 		3,002.7.0.00			
***FOREIGN APPLICATIONS VERIFIED: ***TOREIGN APPLICATIONS VERIFIED: ***Loke PG-PUB DO NOT PUBLISH ** PG-PUB DO NOT PUB		HTLE : Planar simplification	transistor structi	ure using isc	olation implants	for impro				
*** FOREIGN APPLICATIONS VERIFIED: **** **** *** *** *** *** ***		Verified and Ackno	owledged Examiners	's intials λ	cke					
CONTINUING DATA VERIFIED: *CONTINUING DATA VERIFIED: ******Coke ****Loke *****FOREIGN APPLICATIONS VERIFIED: ***********************************				□ yes	s M no		ATTORNEY D	OCKET	NO	
**CONTINUING DATA VERIFIED: Time: Loke **FOREIGN APPLICATIONS VERIFIED:		PG-PUB DO I	NOT PUBLISH							
"**CONTINUING DATA VERIFIED: Time: Loke **FOREIGN APPLICATIONS VERIFIED: Time: Ti	į		NAME OF THE OWNER O		وأوائه المعاورة	~~~				
**CONTINUING DATA VERIFIED: **Continuing Dat										
**APPLICANTS: Randolph Mark; **CONTINUING DATA VERIFIED:	۱, ا	** FOREIGN APPLICATIONS VERIFIED:								
**APPLICANTS: Randolph Mark; **CONTINUING DATA VERIFIED:										,
**APPLICANTS: Randolph Mark; **CONTINUING DATA VERIFIED: **TURE.	1									
**APPLICANTS: Randolph Mark; **CONTINUING DATA VERIFIED: **TURE.										
**APPLICANTS: Randolph Mark; **CONTINUING DATA VERIFIED: **TURE.							•			
**APPLICANTS: Randolph Mark; **CONTINUING DATA VERIFIED: **TURE:	ŀ									
**APPLICANTS: Randolph Mark; **CONTINUING DATA VERIFIED:										
**APPLICANTS: Randolph Mark; **CONTINUING DATA VERIFIED: **TURE.										
**APPLICANTS: Randolph Mark; **CONTINUING DATA VERIFIED:										
		u	IG DATA VERIF	IED:						
				. ,						
L 10032646 12/27/2001 257 374 2811				257 dolph Mark;	374	2811				